*ASSP*

# Single Serial Input PLL Frequency Synthesizer On-chip 1.2 GHz Prescaler

# MB15E03SL

## ■ DESCRIPTION

The Fujitsu MB15E03SL is a serial input Phase Locked Loop (PLL) frequency synthesizer with a 1.2 GHz prescaler. The 1.2 GHz prescaler has a dual modulus division ratio of 64/65 or 128/129 enabling pulse swallowing operation.

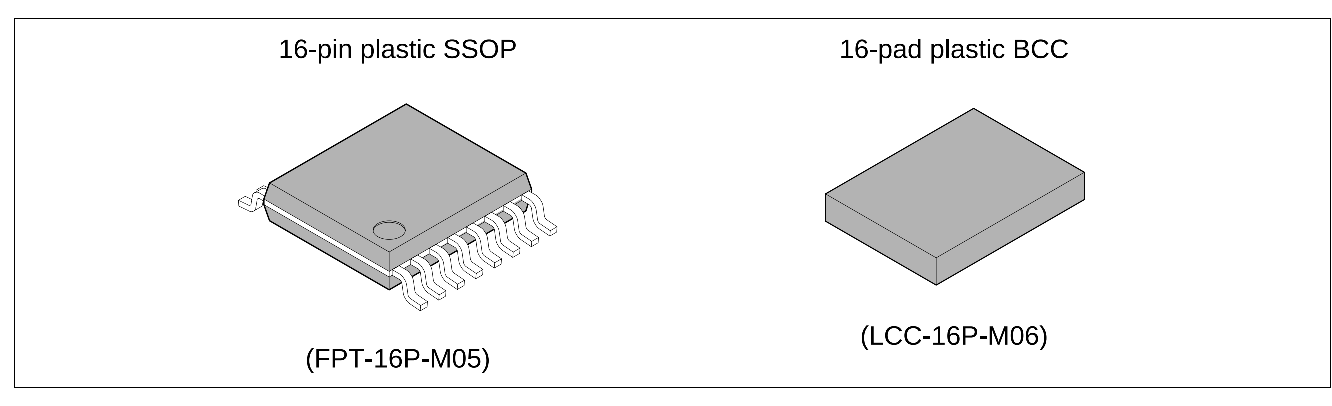
The supply voltage range is between 2.4 V and 3.6 V. The MB15E03SL uses the latest BiCMOS process, as a result, the supply current is typically 2.0 mA at 2.7 V. A refined charge pump supplies a well balanced output currents of 1.5 mA or 6 mA. The charge pump current is selectable by serial data.

MB15E03SL is ideally suited for wireless mobile communications, such as GSM.

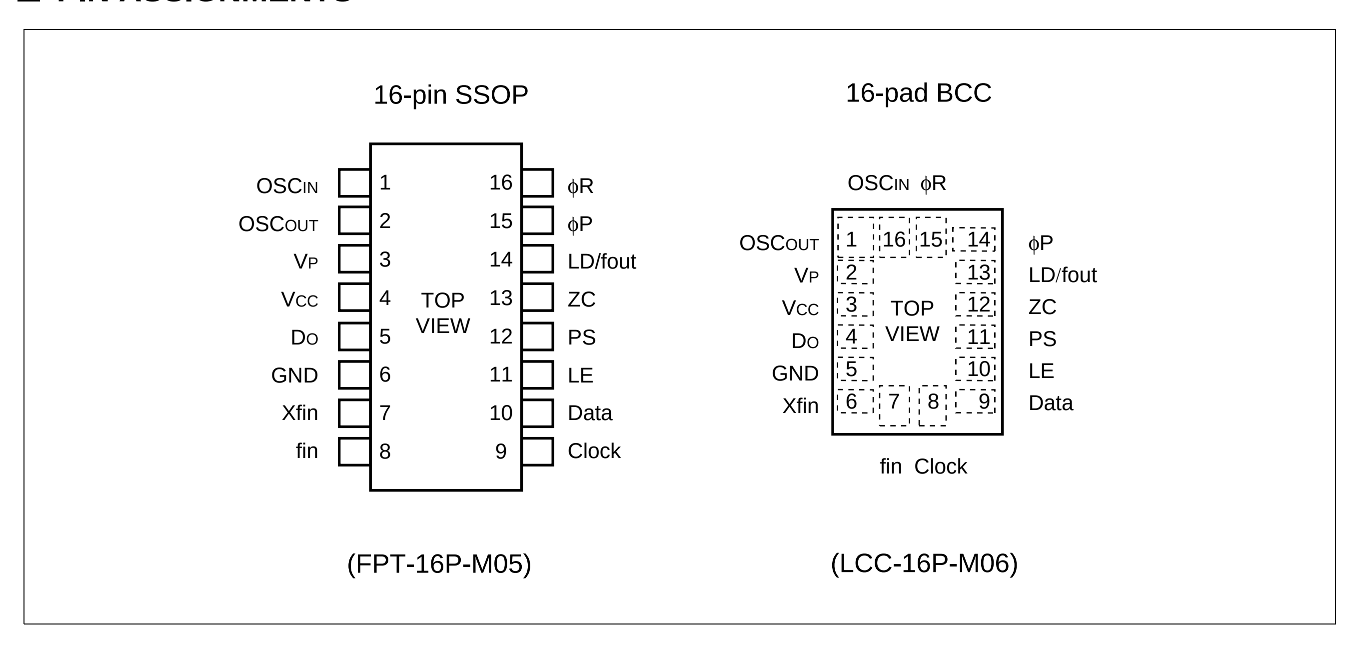
## ■ FEATURES

- High frequency operation: 1.2 GHz max
- Low power supply voltage: $V_{CC}$ = 2.4 V to 3.6 V
- Ultra Low power supply current: $I_{CC}$ = 2.0 mA typ. ($V_{CC}$ = Vp = 2.7 V, Ta = +25°C, in locking state)
  $I_{CC}$ = 2.5 mA typ. ($V_{CC}$ = Vp = 3 V, Ta = +25°C, in locking state)
- Direct power saving function: Power supply current in power saving mode
  Typ. 0.1 µA ($V_{CC}$ = Vp = 3 V, Ta = +25°C), Max. 10 µA ($V_{CC}$ = Vp = 3 V)
- Dual modulus prescaler: 64/65 or 128/129
- Serial input 14-bit programmable reference divider: R = 3 to 16,383
- Serial input programmable divider consisting of:
  - Binary 7-bit swallow counter: 0 to 127
  - Binary 11-bit programmable counter: 3 to 2,047
- Selectable charge pump current
- On-chip phase control for phase comparator
- Operating temperature: Ta = –40 to +85°C
- Pin compatible with MB15E03, MB15E03L

## ■ PACKAGES



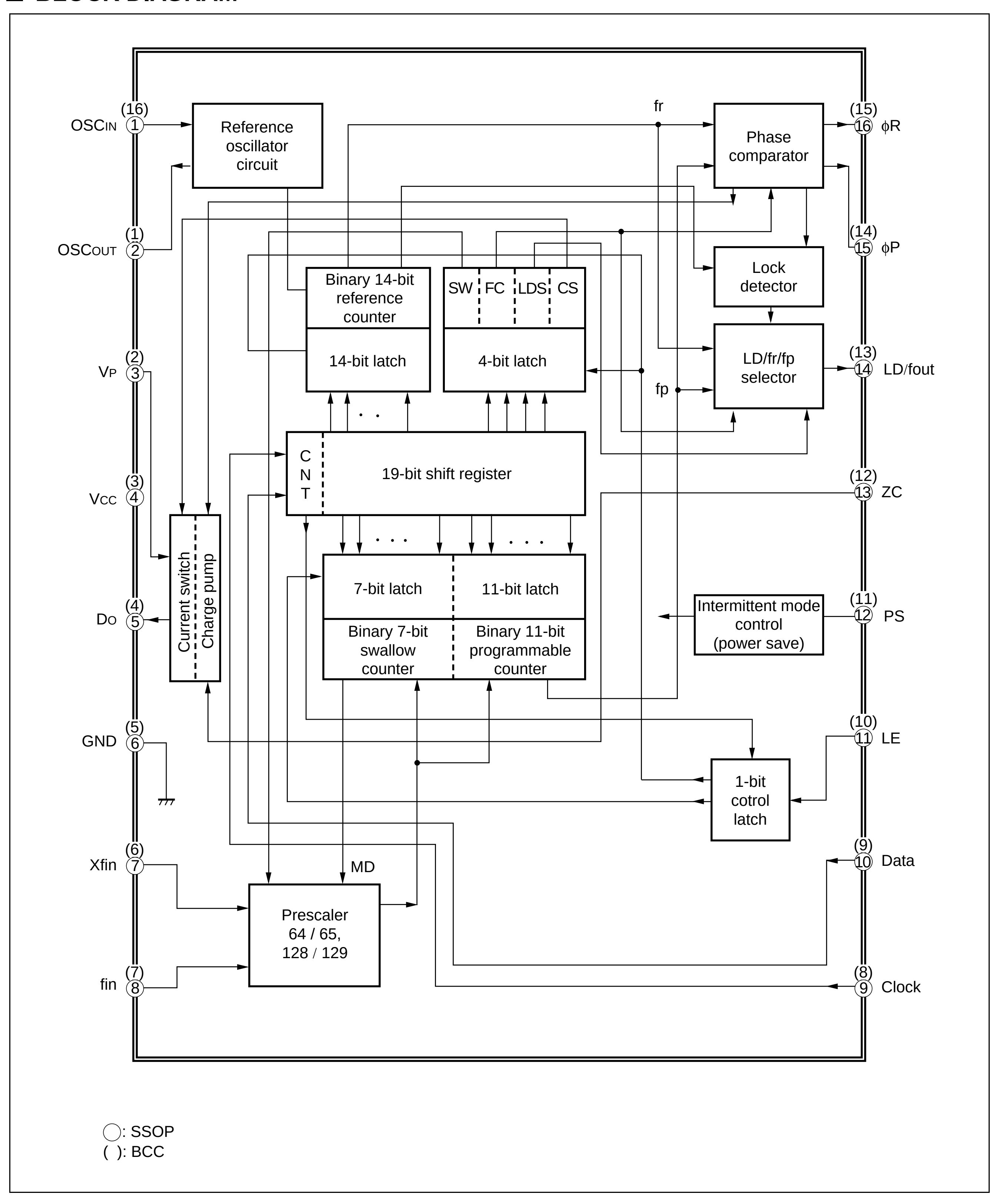
## ■ PIN ASSIGNMENTS



## ■ PIN DESCRIPTION

| Pin No. | | Pin Name | I/O | Descriptions |
|---|---|---|---|---|
| SSOP-16 | BCC-16 | | | |
| 1 | 16 | $OSC_{IN}$ | I | Programmable reference divider input.<br>Oscillator input connection to a TCXO. |
| 2 | 1 | $OSC_{OUT}$ | O | Oscillator output. |
| 3 | 2 | $V_P$ | — | Power supply voltage input for the charge pump. |
| 4 | 3 | $V_{CC}$ | — | Power supply voltage input. |
| 5 | 4 | $D_O$ | O | Charge pump output.<br>Phase of the charge pump can be selected via programming of the FC bit. |
| 6 | 5 | GND | — | Ground. |
| 7 | 6 | Xfin | I | Prescaler complementary input which should be grounded via a capacitor. |
| 8 | 7 | fin | I | Prescaler input.<br>Connection to an external VCO should be done via AC coupling. |
| 9 | 8 | Clock | I | Clock input for the 19-bit shift register.<br>Data is shifted into the shift register on the rising edge of the clock.<br>(Open is prohibited.) |
| 10 | 9 | Data | I | Serial data input using binary code.<br>The last bit of the data is a control bit. (Open is prohibited.) |
| 11 | 10 | LE | I | Load enable signal input. (Open is prohibited.)<br>When LE is set high, the data in the shift register is transferred to a latch according to the control bit in the serial data. |
| 12 | 11 | PS | I | Power saving mode control. This pin must be set at “L” at Power-ON. (Open is prohibited.)<br>PS = “H”; Normal mode<br>PS = “L”; Power saving mode |
| 13 | 12 | ZC | I | Forced high-impedance control for the charge pump (with internal pull up resistor.)<br>ZC = “H”; Normal Do output.<br>ZC = “L”; Do becomes high impedance. |
| 14 | 13 | LD/fout | O | Lock detect signal output (LD)/phase comparator monitoring output (fout).<br>The output signal is selected via programming of the LDS bit.<br>LDS = “H”; outputs fout (fr/fp monitoring output)<br>LDS = “L”; outputs LD (“H” at locking, “L” at unlocking.) |
| 15 | 14 | $\phi$P | O | Phase comparator N-channel open drain output for an external charge pump. Phase can be selected via programming of the FC bit. |
| 16 | 15 | $\phi$R | O | Phase comparator CMOS output for an external charge pump. Phase can be selected via programming of the FC bit. |

## ■ BLOCK DIAGRAM



## ■ ABSOLUTE MAXIMUM RATINGS

| Parameter | Symbol | Condition | Rating | | Unit | Remark |
|---|---|---|---|---|---|---|
| | | | Min. | Max. | | |
| Power supply voltage | $V_{CC}$ | — | –0.5 | 4.0 | V | |
| | $V_P$ | — | $V_{CC}$ | 6.0 | V | |
| Input voltage | $V_I$ | — | –0.5 | $V_{CC}$ +0.5 | V | |
| Output voltage | $V_O$ | Except Do | GND | $V_{CC}$ | V | |
| | $V_O$ | Do | GND | $V_P$ | V | |
| Storage temperature | Tstg | — | –55 | +125 | °C | |

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

## ■ RECOMMENDED OPERATING CONDITIONS

| Parameter | Symbol | Value | | | Unit | Remark |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Power supply voltage | $V_{CC}$ | 2.4 | 3.0 | 3.6 | V | |
| | $V_P$ | $V_{CC}$ | — | 5.5 | V | |
| Input voltage | $V_I$ | GND | — | $V_{CC}$ | V | |
| Operating temperature | Ta | –40 | — | +85 | °C | |

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

## ■ ELECTRICAL CHARACTERISTICS

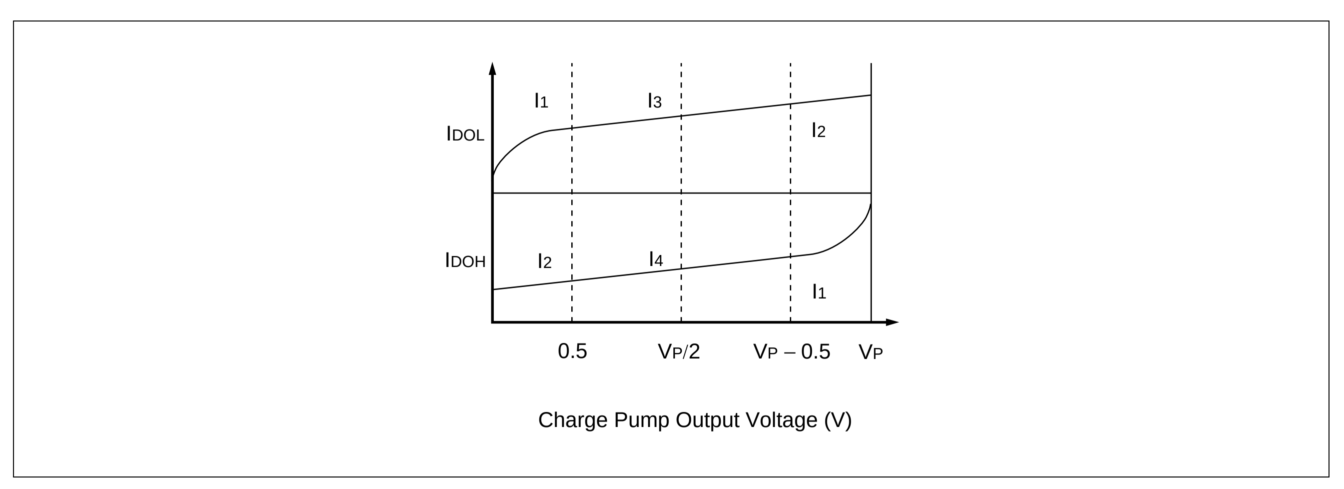
($V_{CC}$ = 2.4 to 3.6 V, Ta = –40 to +85°C)

| Parameter | | Symbol | Condition | Value Min. | Value Typ. | Value Max. | Unit |
|---|---|---|---|---|---|---|---|
| Power supply current*1 | | $I_{CC}$ | $V_{CC} = V_P$ = 2.7 V ($V_{CC} = V_P$ = 3.0 V) | — | 2.0 (2.5) | — | mA |
| Power saving current | | $I_{PS}$ | ZC = “H” or open | — | 0.1*2 | 10 | µA |
| Operating frequency | fin | fin | — | 100 | — | 1200 | MHz |
| | $OSC_{IN}$ | $f_{OSC}$ | — | 3 | — | 40 | MHz |
| Input sensitivity | fin*3 | Pfin | 50 Ω system (Refer to the Measurment circuit.) | –15 | — | +2 | dBm |
| | $OSC_{IN}$*3 | $V_{OSC}$ | — | 0.5 | — | $V_{CC}$ | Vp-p |
| “H” level input voltage | Data, Clock, LE, PS, ZC | $V_{IH}$ | — | $V_{CC}$ × 0.7 | — | — | V |
| “L” level input voltage | | $V_{IL}$ | — | — | — | $V_{CC}$ × 0.3 | |
| “H” level input current | Data, Clock, LE, PS | $I_{IH}$*4 | — | –1.0 | — | +1.0 | µA |
| “L” level input current | | $I_{IL}$*4 | — | –1.0 | — | +1.0 | |
| “H” level input current | $OSC_{IN}$ | $I_{IH}$ | — | 0 | — | +100 | µA |
| “L” level input current | | $I_{IL}$*4 | — | –100 | — | 0 | |
| “H” level input current | ZC | $I_{IH}$*4 | — | –1.0 | — | +1.0 | µA |
| “L” level input current | | $I_{IL}$*4 | Pull up input | –100 | — | 0 | |
| “L” level output voltage | φP | $V_{OL}$ | Open drain output | — | — | 0.4 | V |
| “H” level output voltage | φR, LD/fout | $V_{OH}$ | $V_{CC} = V_P$ = 3 V, $I_{OH}$ = –1 mA | $V_{CC}$ – 0.4 | — | — | V |
| “L” level output voltage | | $V_{OL}$ | $V_{CC} = V_P$ = 3 V, $I_{OL}$ = 1 mA | — | — | 0.4 | |
| “H” level output voltage | Do | $V_{DOH}$ | $V_{CC} = V_P$ = 3 V, $I_{DOH}$ = –0.5 mA | $V_P$ – 0.4 | — | — | V |
| “L” level output voltage | | $V_{DOL}$ | $V_{CC} = V_P$ = 3 V, $I_{DOL}$ = 0.5 mA | — | — | 0.4 | |
| High impedance cutoff current | Do | $I_{OFF}$ | $V_{CC} = V_P$ = 3 V, $V_{OFF}$ = 0.5 V to $V_P$ – 0.5 V | — | — | 2.5 | nA |
| “L” level output current | φP | $I_{OL}$ | Open drain output | 1.0 | — | — | mA |
| “H” level output current | φR, LD/fout | $I_{OH}$ | — | — | — | –1.0 | mA |
| “L” level output current | | $I_{OL}$ | — | 1.0 | — | — | |
| “H” level output current | Do | $I_{DOH}$*4 | $V_{CC}$ = 3 V, $V_P$ = 3 V, $V_{DO} = V_P/2$, Ta = +25°C; CS bit = “H” | — | –6.0 | — | mA |
| | | | CS bit = “L” | — | –1.5 | — | |
| “L” level output current | | $I_{DOL}$ | CS bit = “H” | — | 6.0 | — | |
| | | | CS bit = “L” | — | 1.5 | — | |
| Charge pump current rate | $I_{DOL}/I_{DOH}$ | $I_{DOMT}$*5 | $V_{DD} = V_P/2$ | — | 3 | — | % |
| | vs $V_{DO}$ | $I_{DOVD}$*6 | 0.5 V ≤ $V_{DO}$ ≤ $V_P$ – 0.5 V | — | 10 | — | % |
| | vs Ta | $I_{DOTA}$*7 | – 40°C ≤ Ta ≤ +85°C | — | 10 | — | % |

*(Continued)*

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*1: Conditions; fin = 1200 MHz, fosc = 12 MHz, Ta = +25°C, in locking state.
*2: $V_{CC} = V_P$ = 3.0 V, fosc = 12.8 MHz, Ta = +25°C, in power saving mode
*3: AC coupling. 1000 pF capacitor is connected under the condition of min. operating frequency.
*4: The symbol "–" (minus) means direction of current flow.
*5: $V_{CC} = V_P$ = 3.0 V, Ta = +25°C $(|I_3| - |I_4|) / [(|I_3| + |I_4|) /2] \times 100(\%)$
*6: $V_{CC} = V_P$ = 3.0 V, Ta = +25°C $[(|I_2| - |I_1|) /2] / [(|I_1| + |I_2|) /2] \times 100(\%)$ (Applied to each $I_{DOL}$, $I_{DOH}$)
*7: $V_{CC} = V_P$ = 3.0 V, $V_{DO} = V_P/2$ $(|I_{DO(+85°C)} - I_{DO(-40°C)}| /2) / (|I_{DO(+85°C)} + I_{DO(-40°C)}| /2) \times 100(\%)$ (Applied to each $I_{DOL}$, $I_{DOH}$)



## ■ FUNCTIONAL DESCRIPTION

### 1. Pulse Swallow Function

The divide ratio can be calculated using the following equation:

$f_{VCO} = [(M \times N) + A] \times f_{OSC} \div R \quad (A < N)$

- $f_{VCO}$ : Output frequency of external voltage controlled oscillator (VCO)
- N : Preset divide ratio of binary 11-bit programmable counter (3 to 2,047)
- A : Preset divide ratio of binary 7-bit swallow counter ($0 \leq A \leq 127$)
- $f_{OSC}$ : Output frequency of the reference frequency oscillator
- R : Preset divide ratio of binary 14-bit programmable reference counter (3 to 16,383)
- M : Preset divide ratio of the dual modulus prescaler (64 or 128)

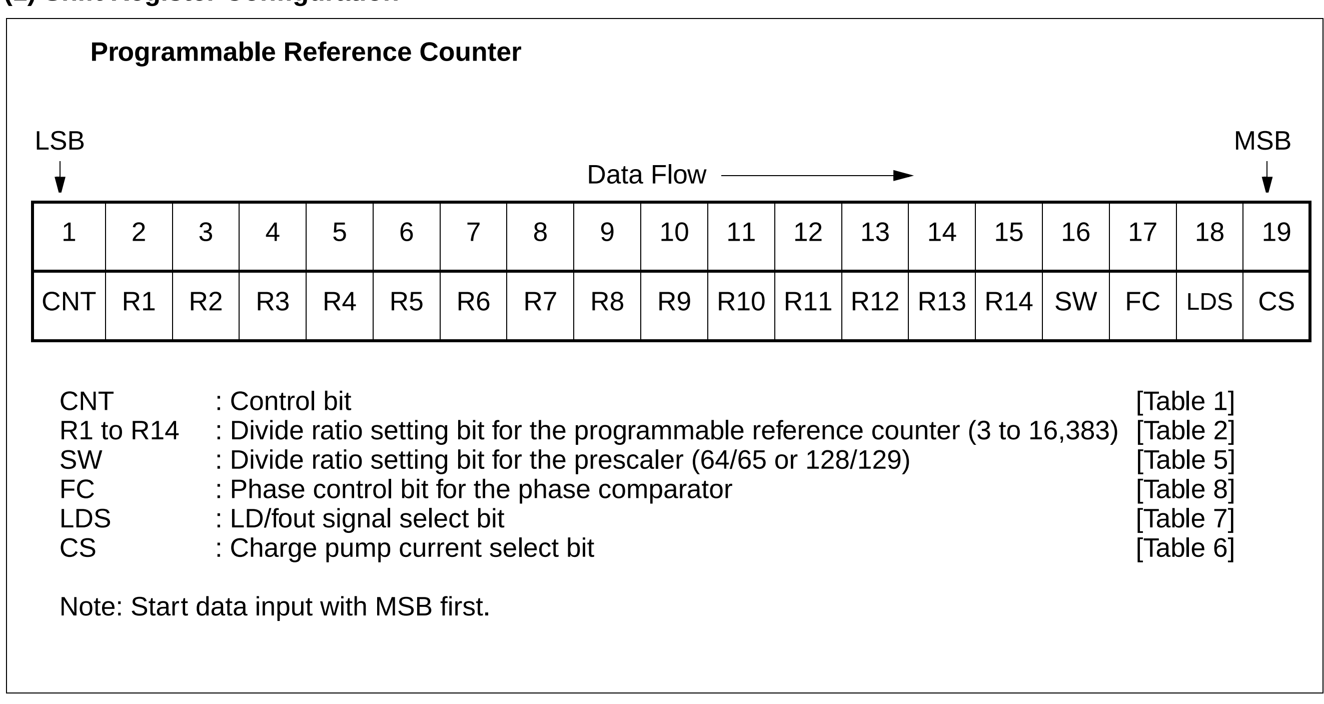
### 2. Serial Data Input

Serial data is processed using the Data, Clock, and LE pins. Serial data controls the programmable reference divider and the programmable divider separately.
Binary serial data is entered through the Data pin.
One bit of data is shifted into the shift register on the rising edge of the Clock. When the LE pin is taken high, stored data is latched according to the control bit data as follows:

**Table 1. Control Bit**

| Control Bit (CNT) | Destination of Serial Data |
|---|---|
| H | For the programmable reference divider |
| L | For the programmable divider |

**(1) Shift Register Configuration**



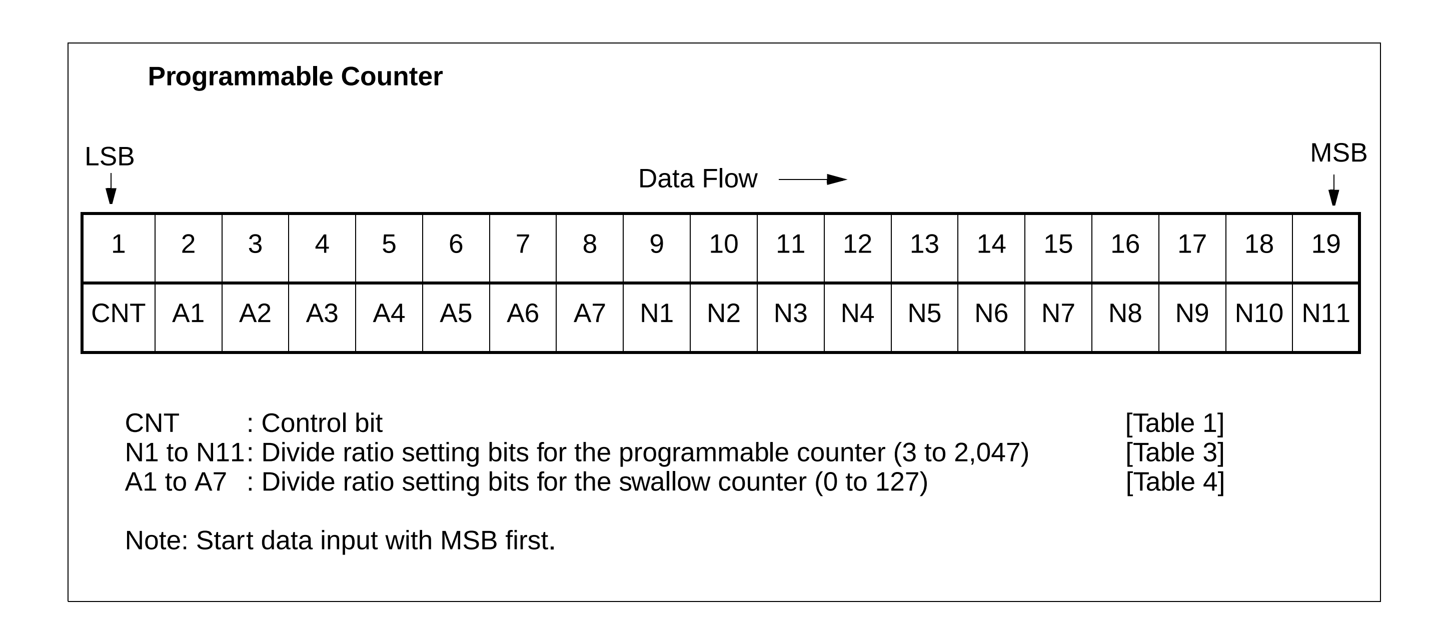



**Table 2. Binary 14-bit Programmable Reference Counter Data Setting**

| Divide ratio (R) | R14 | R13 | R12 | R11 | R10 | R9 | R8 | R7 | R6 | R5 | R4 | R3 | R2 | R1 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 3 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| 4 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| · | · | · | · | · | · | · | · | · | · | · | · | · | · | · |
| 16383 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

Note: Divide ratio less than 3 is prohibited.

**Table 3. Binary 11-bit Programmable Counter Data Setting**

| Divide ratio (N) | N11 | N10 | N9 | N8 | N7 | N6 | N5 | N4 | N3 | N2 | N1 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 3 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| 4 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| · | · | · | · | · | · | · | · | · | · | · | · |
| 2047 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

Note: Divide ratio less than 3 is prohibited.

### Table 4. Binary 7-bit Swallow Counter Data Setting

| Divide ratio (A) | A7 | A6 | A5 | A4 | A3 | A2 | A1 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| · | · | · | · | · | · | · | · |
| 127 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

### Table 5. Prescaler Data Setting

| SW | Prescaler Divide Ratio |
|---|---|
| H | 64/65 |
| L | 128/129 |

### Table 6. Charge Pump Current Setting

| CS | Current Value |
|---|---|
| H | ±6.0 mA |
| L | ±1.5 mA |

### Table 7. LD/fout Output Select Data Setting

| LDS | LD/$f_{OUT}$ Output Signal |
|---|---|
| H | fout signal |
| L | LD signal |

#### (2) Relation between the FC Input and Phase Characteristics

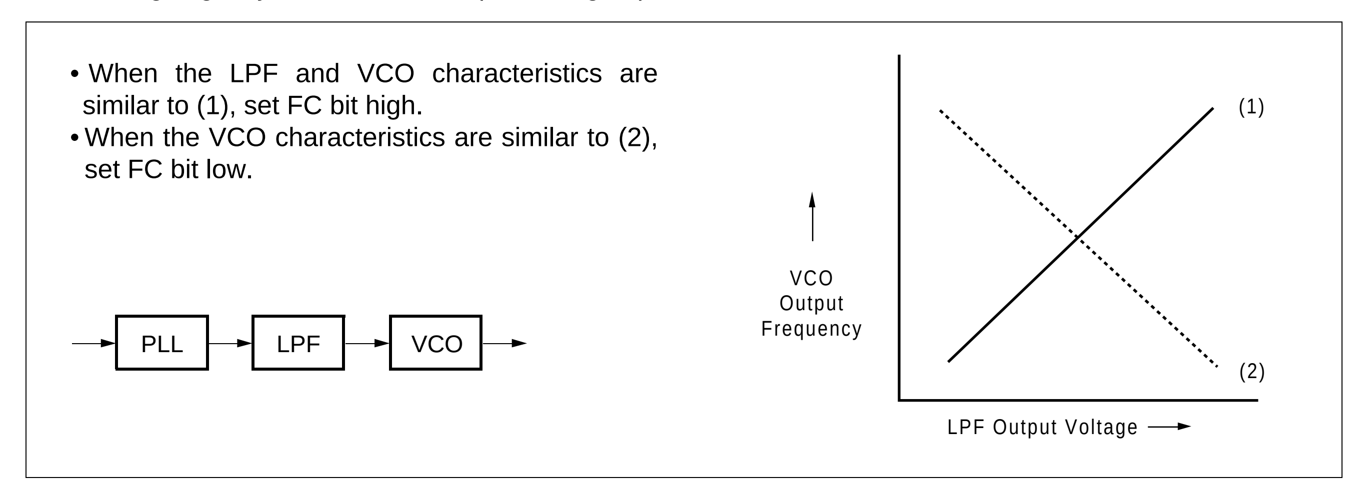
The FC bit changes the phase characteristics of the phase comparator. Both the internal charge pump output level ($D_O$) and the phase comparator output (ϕR, ϕP) are reversed according to the FC bit. Also, the monitor pin (fout) output is controlled by the FC bit. The relationship between the FC bit and each of $D_O$, ϕR, and ϕP is shown below.

### Table 8. FC Bit Data Setting (LDS = “H”)

| | FC = High | | | | FC = Low | | | |
|---|---|---|---|---|---|---|---|---|
| | $D_O$ | ϕR | ϕP | LD/fout | $D_O$ | ϕR | ϕP | LD/fout |
| fr > fp | H | L | L | fout = fr | L | H | Z* | fout = fp |
| fr < fp | L | H | Z* | | H | L | L | |
| fr = fp | Z* | L | Z* | | Z* | L | Z* | |

* : High impedance

When designing a synthesizer, the FC pin setting depends on the VCO and LPF characteristics.




### 3. Do Output Control

**Table 9. ZC Pin Setting**

| ZC pin | Do output |
| --- | --- |
| H | Normal output |
| L | High impedance |

## 4. Power Saving Mode (Intermittent Mode Control Circuit)

### Table 10. PS Pin Setting

| PS pin | Status |
|---|---|
| H | Normal mode |
| L | Power saving mode |

The intermittent mode control circuit reduces the PLL power consumption.

By setting the PS pin low, the device enters into the power saving mode, reducing the current consumption. See the Electrical Characteristics chart for the specific value.

The phase detector output, Do, becomes high impedance.

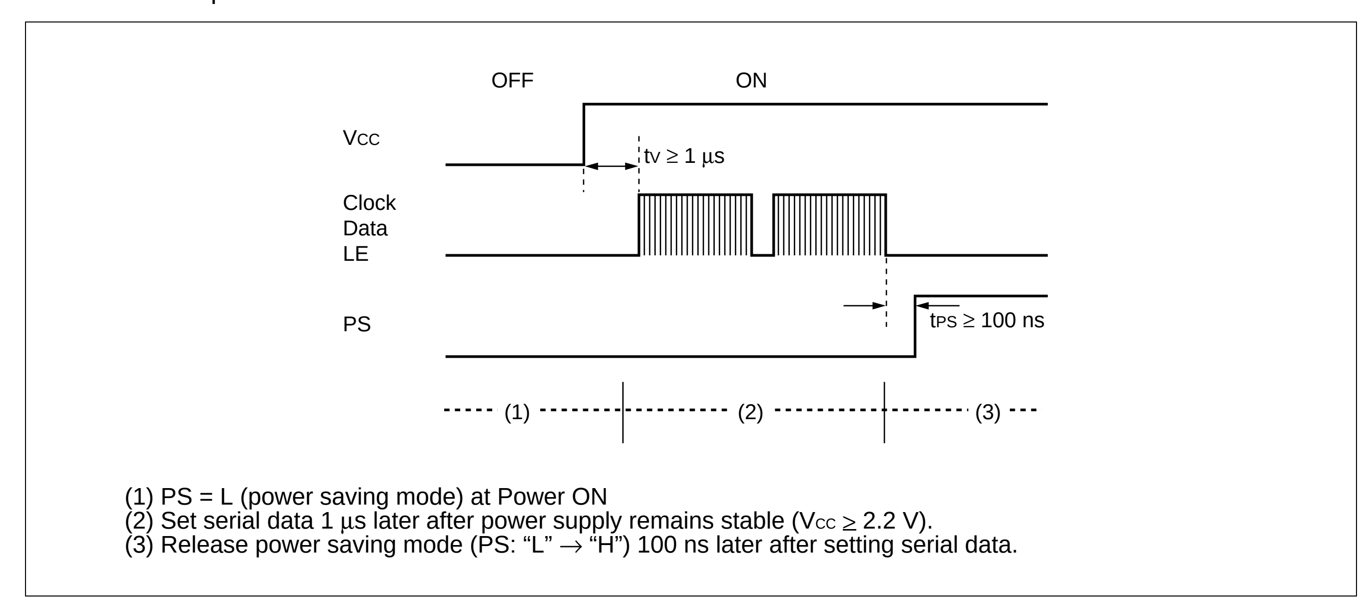
For the signal PLL, the lock detector, LD, remains high, indicating a locked condition.

Setting the PS pin high, releases the power saving mode, and the device works normally.

The intermittent mode control circuit also ensures a smooth startup when the device returns to normal operation. When the PLL is returned to normal operation, the phase comparator output signal is unpredictable. This is because of the unknown relationship between the comparison frequency (fp) and the reference frequency (fr) which can cause a major change in the comparator output, resulting in a VCO frequency jump and an increase in lockup time.

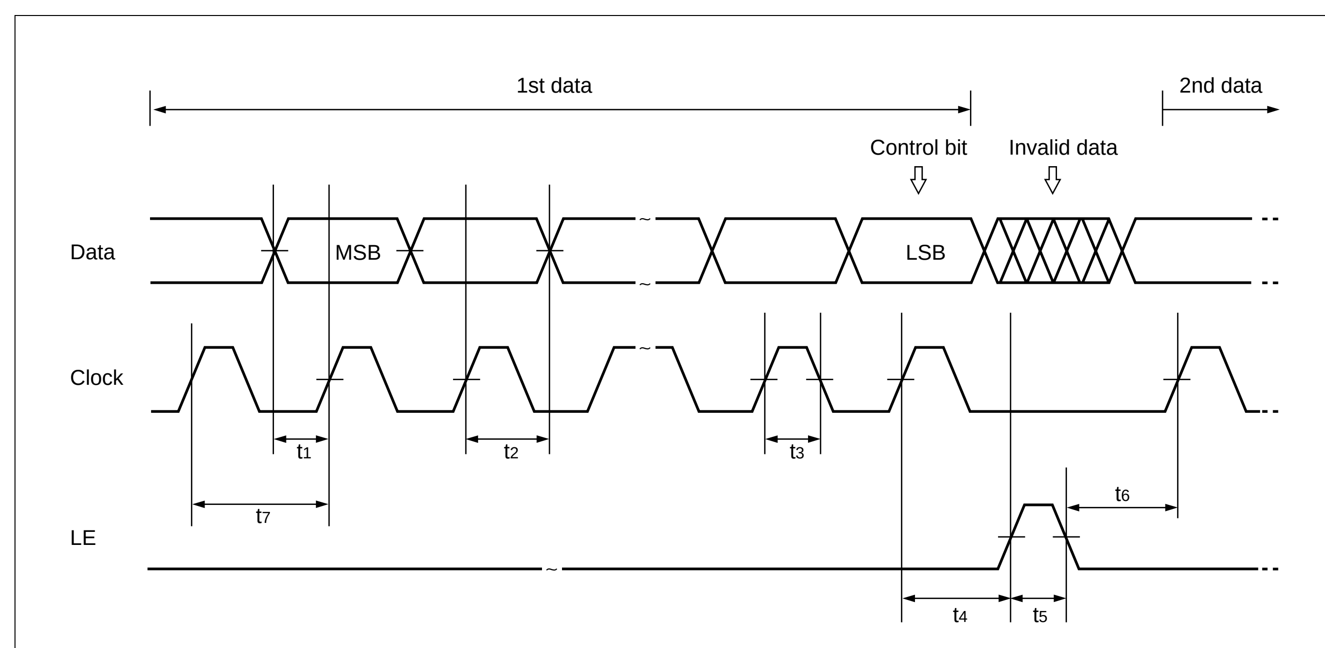
To prevent a major VCO frequency jump, the intermittent mode control circuit limits the magnitude of the error signal from the phase detector when it returns to normal operation.

Notes: •When power ($V_{CC}$) is first applied, the device must be in standby mode, PS = Low, for at least 1 µs.
•PS pin must be set "L" for Power-ON.




(1) PS = L (power saving mode) at Power ON
(2) Set serial data 1 µs later after power supply remains stable ($V_{CC} \geq$ 2.2 V).
(3) Release power saving mode (PS: "L" → "H") 100 ns later after setting serial data.

## ■ SERIAL DATA INPUT TIMING



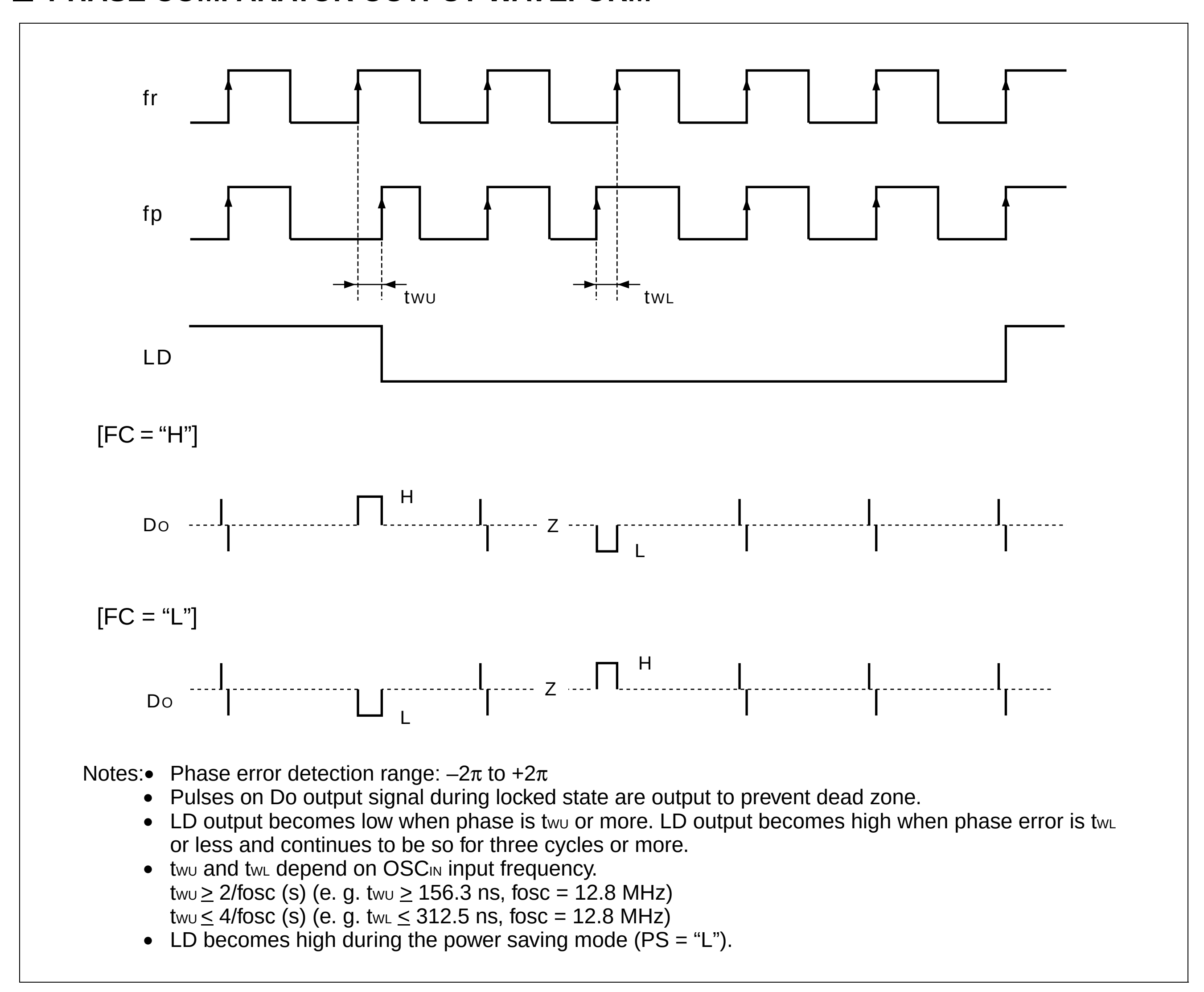

On the rising edge of the clock, one bit of data is transferred into the shift register.

| Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|
| t1 | 20 | — | — | ns |
| t2 | 20 | — | — | ns |
| t3 | 30 | — | — | ns |
| t4 | 30 | — | — | ns |

| Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|
| t5 | 100 | — | — | ns |
| t6 | 20 | — | — | ns |
| t7 | 100 | — | — | ns |

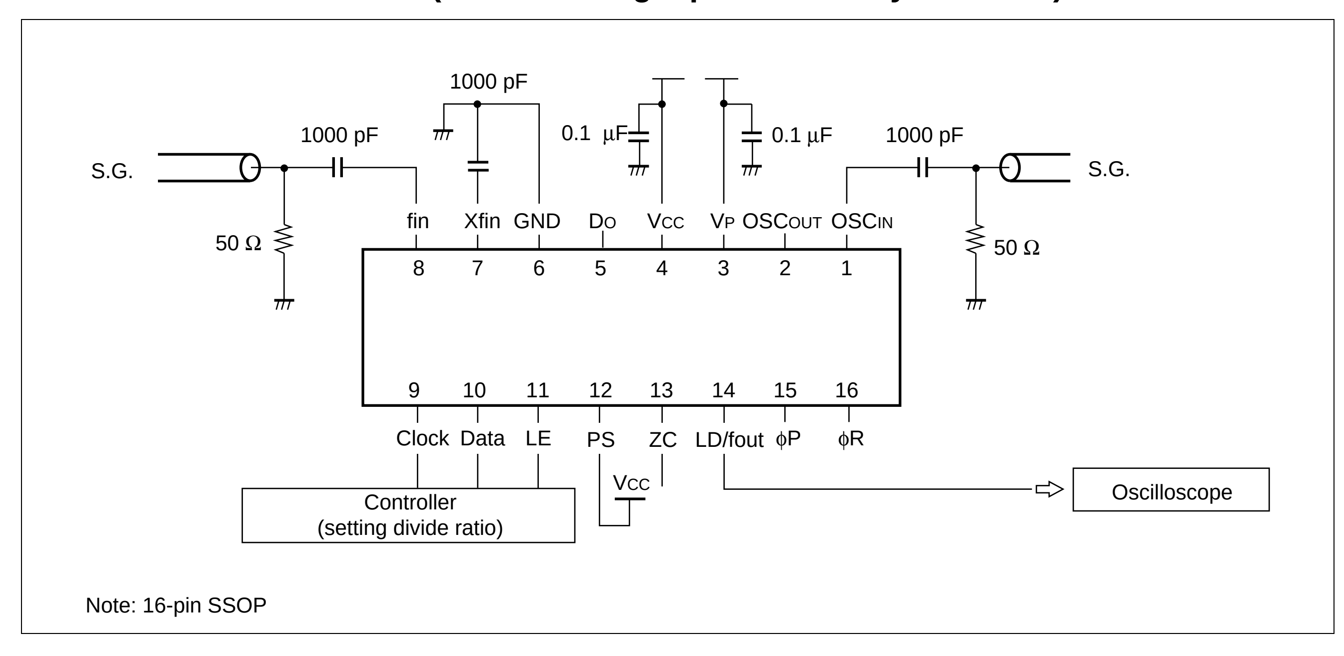
Note: LE should be “L” when the data is transferred into the shift register.

## ■ PHASE COMPARATOR OUTPUT WAVEFORM



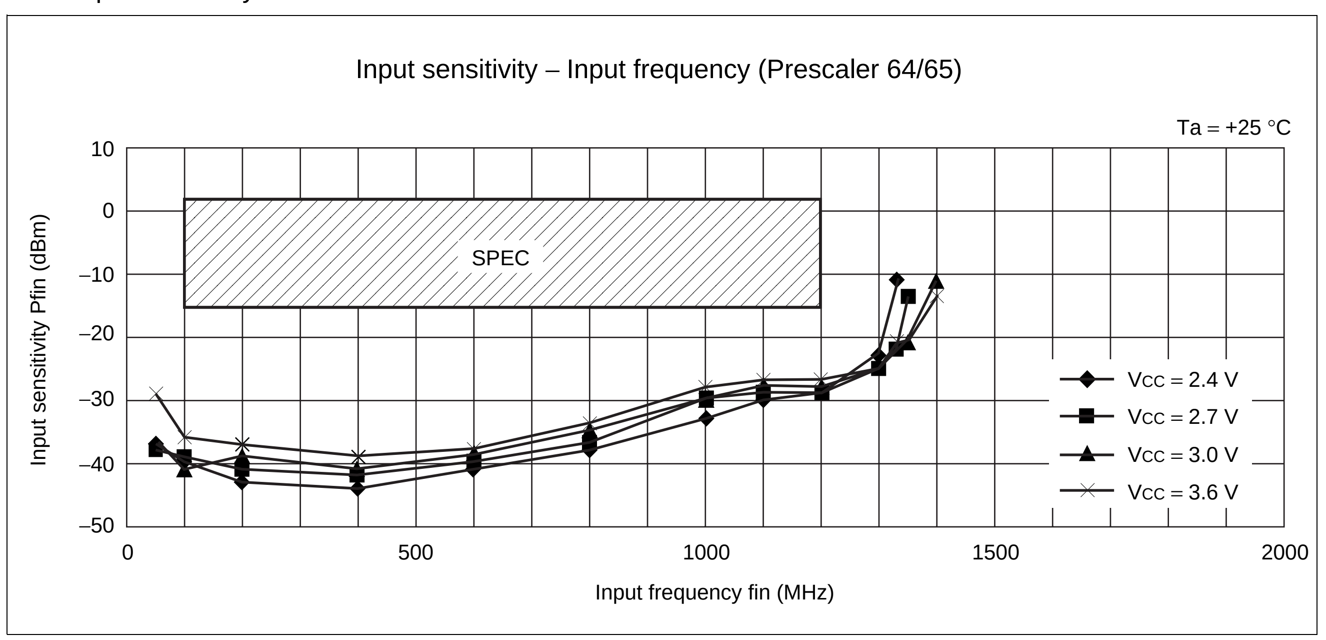

Notes:
- Phase error detection range: –2π to +2π
- Pulses on Do output signal during locked state are output to prevent dead zone.
- LD output becomes low when phase is $t_{WU}$ or more. LD output becomes high when phase error is $t_{WL}$ or less and continues to be so for three cycles or more.
- $t_{WU}$ and $t_{WL}$ depend on $OSC_{IN}$ input frequency.
  $t_{WU} \geq 2/fosc$ (s) (e. g. $t_{WU} \geq 156.3$ ns, fosc = 12.8 MHz)
  $t_{WU} \leq 4/fosc$ (s) (e. g. $t_{WL} \leq 312.5$ ns, fosc = 12.8 MHz)
- LD becomes high during the power saving mode (PS = “L”).

## ■ MEASURMENT CIRCUIT (for Measuring Input Sensitivity fin/OSC$_{IN}$)

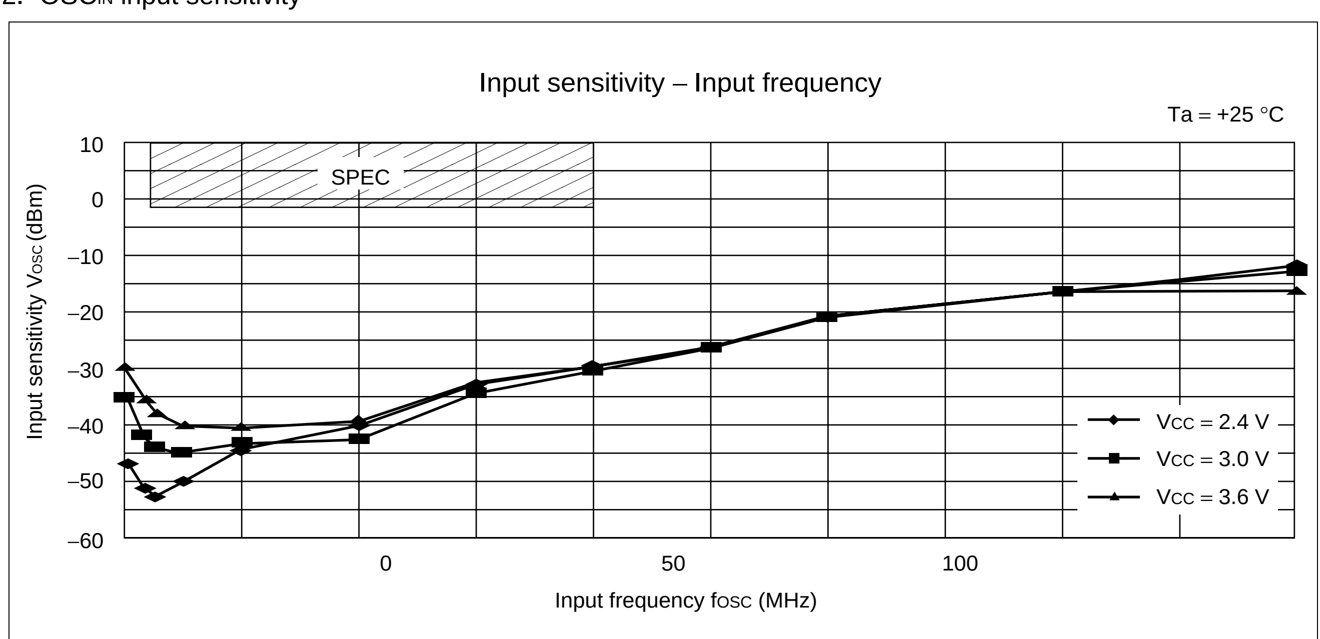


## ■ TYPICAL CHARACTERISTICS

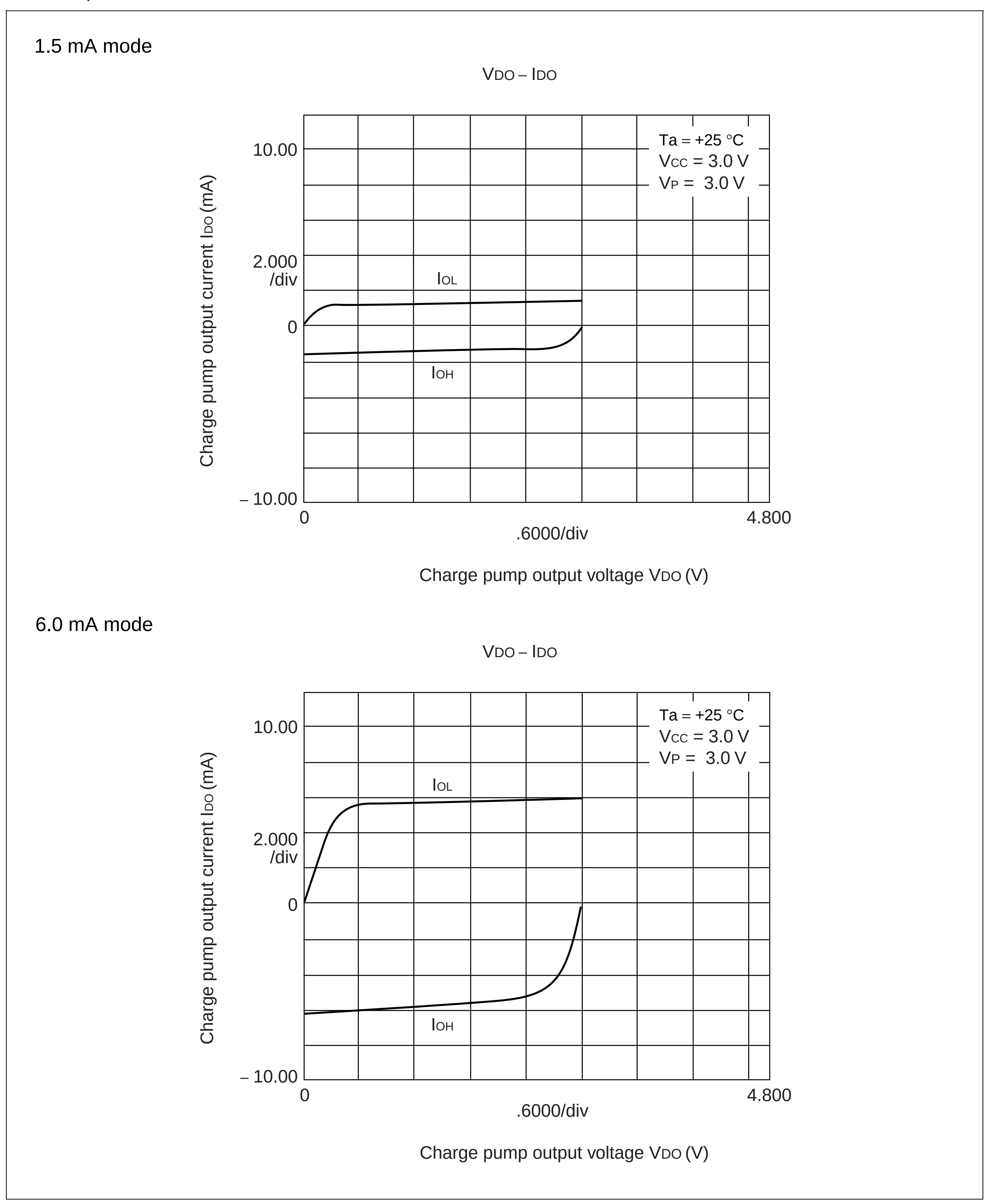
1. fin input sensitivity



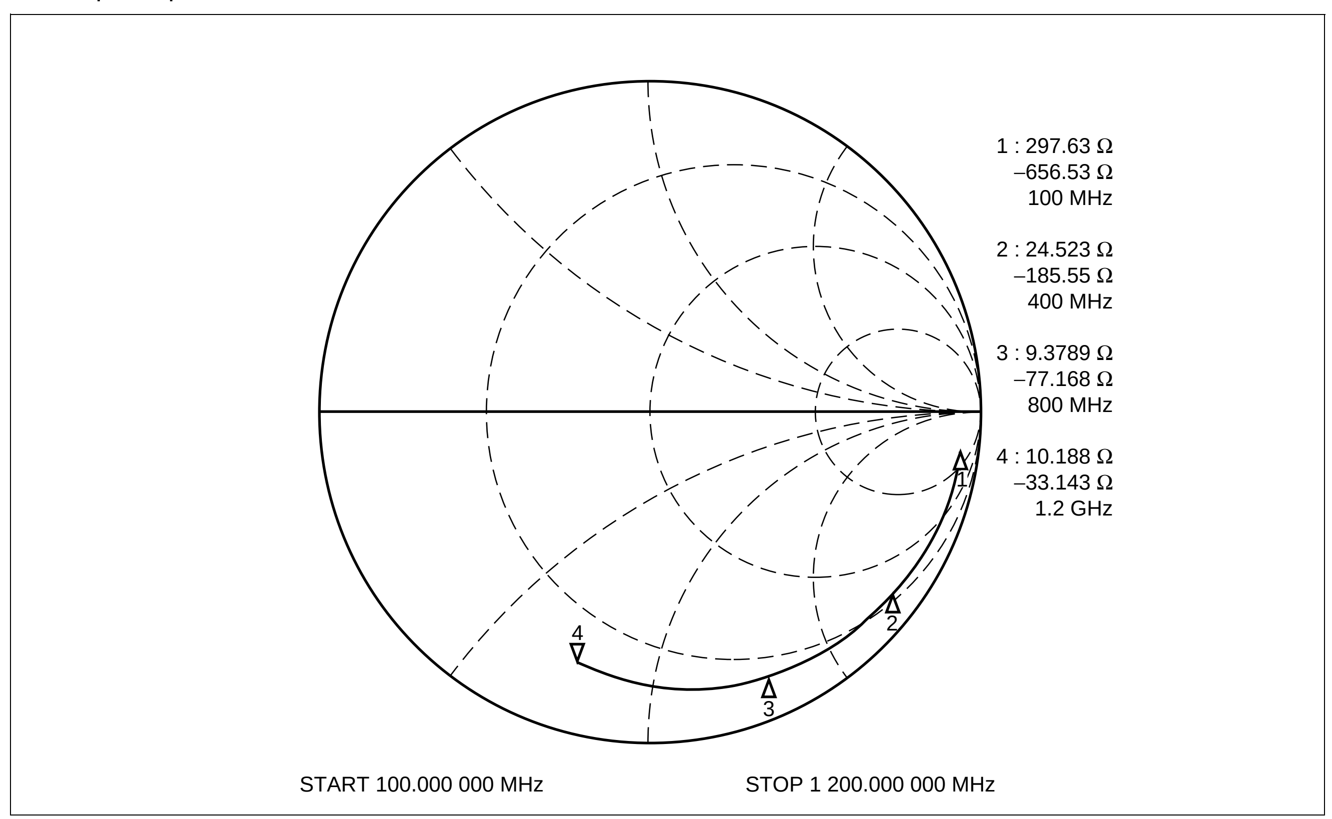

2. $OSC_{IN}$ input sensitivity



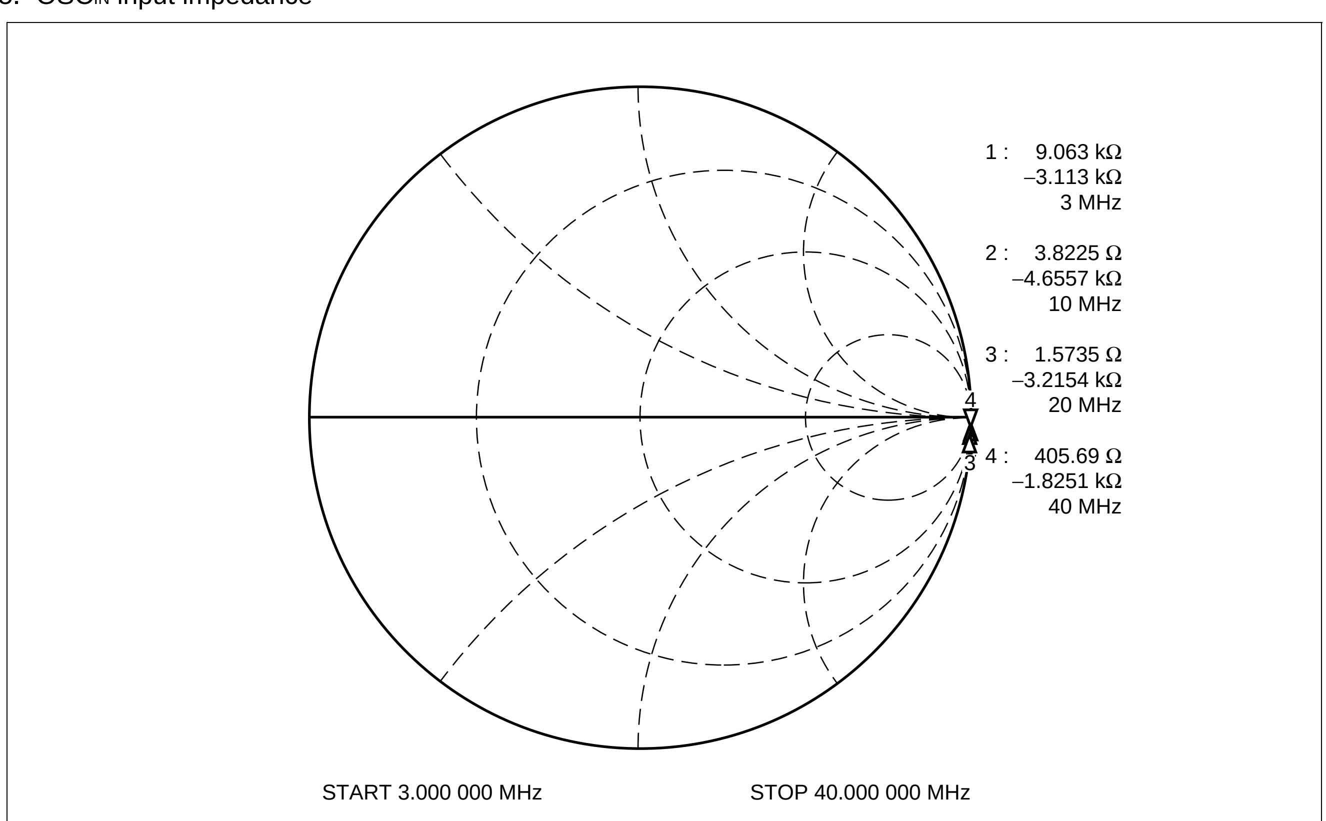
3. Do output current



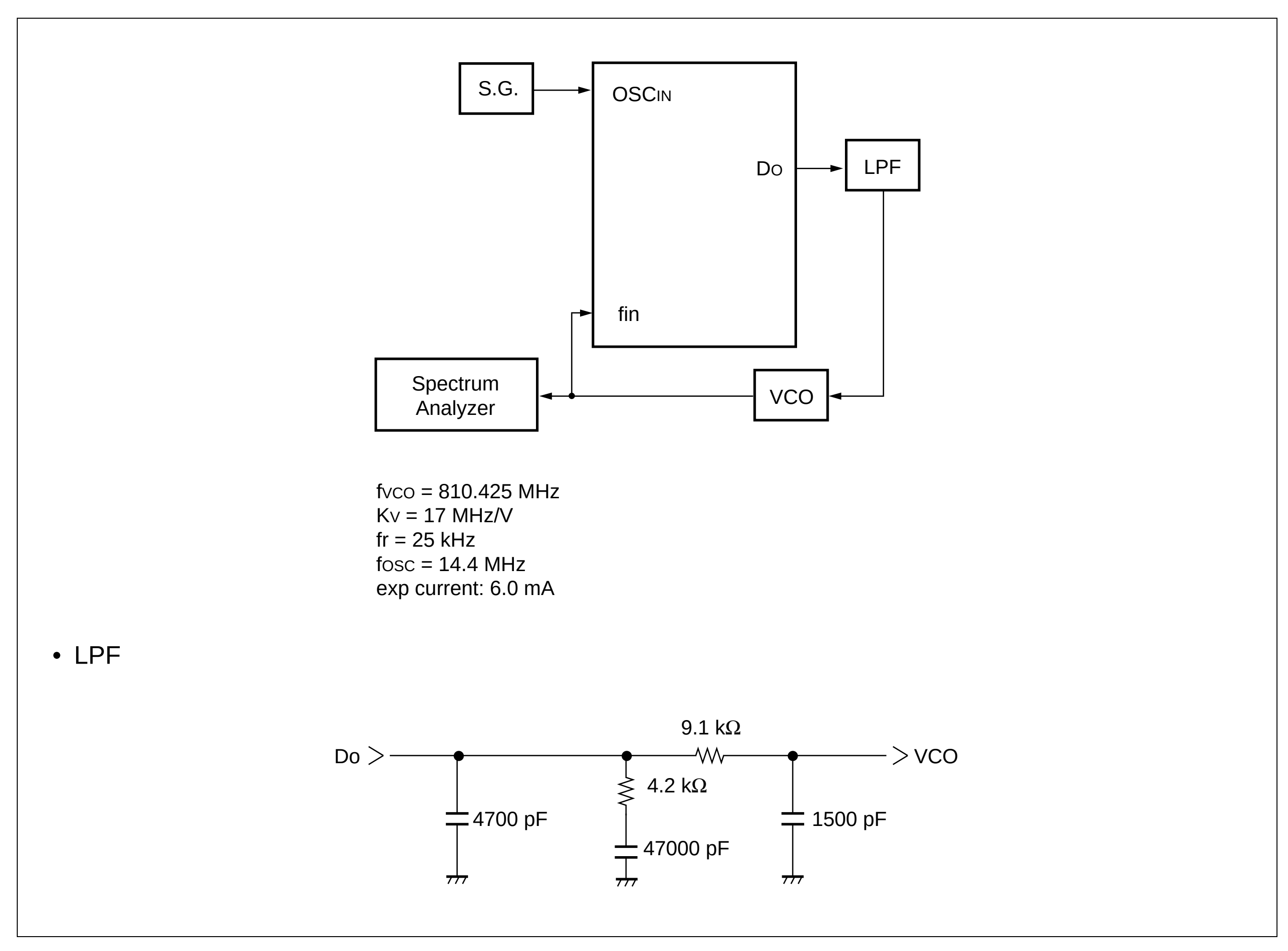
4. fin input impedance



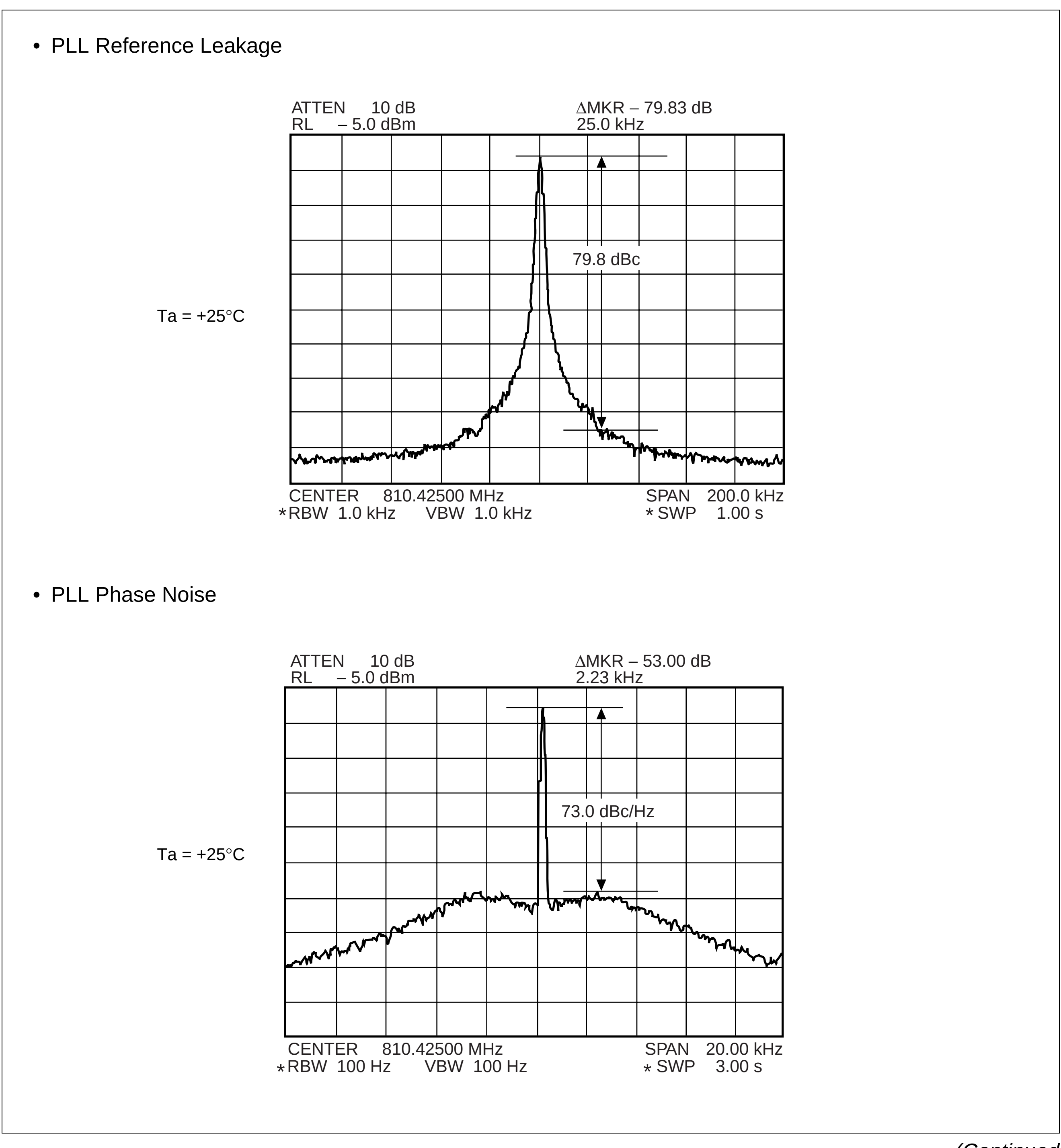

5. OSCIN input impedance



## ■ REFERENCE INFORMATION

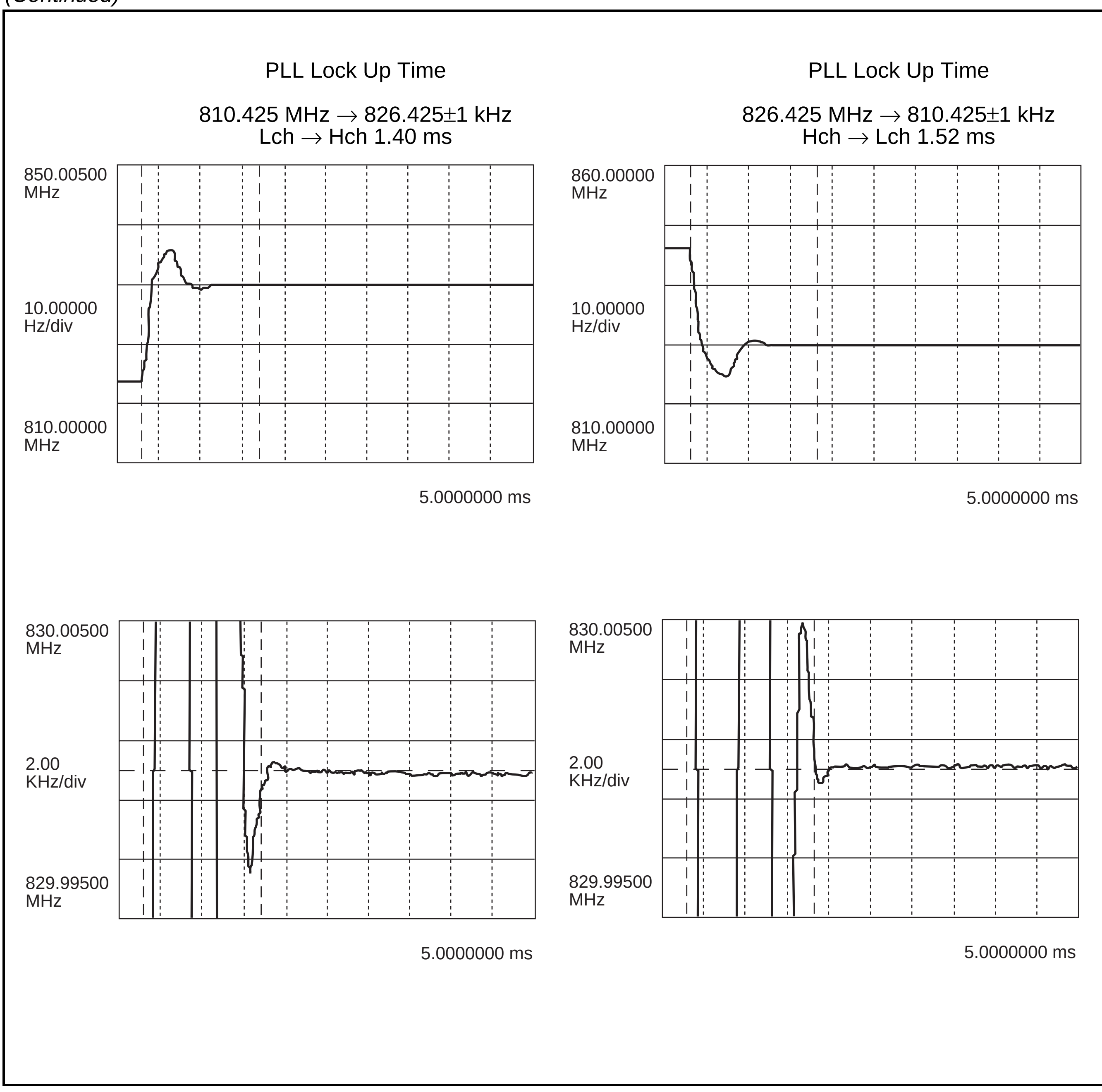



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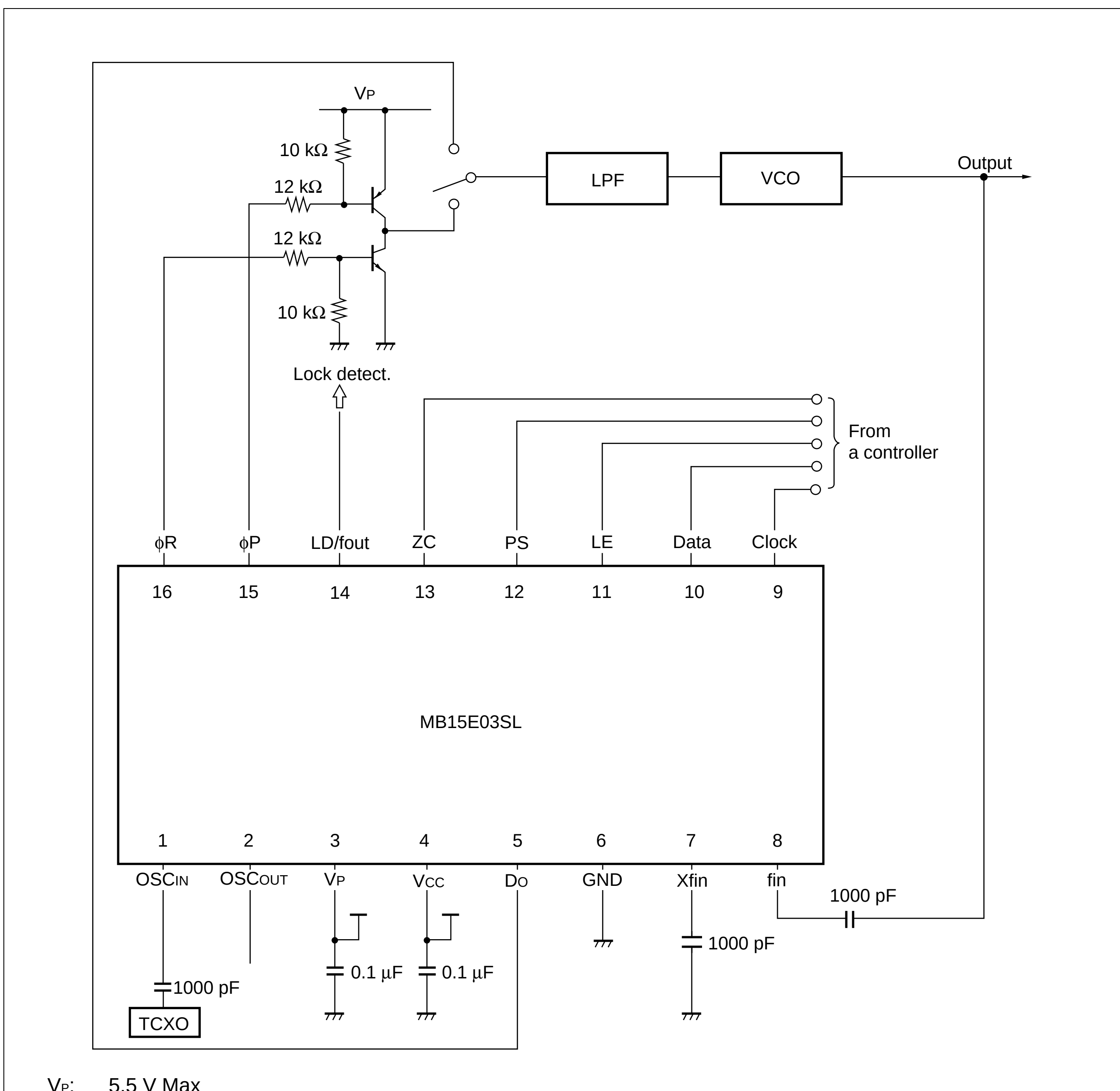

• PLL Reference Leakage
ATTEN 10 dB
RL – 5.0 dBm
ΔMKR – 79.83 dB
25.0 kHz
79.8 dBc
Ta = +25°C
CENTER 810.42500 MHz
*RBW 1.0 kHz VBW 1.0 kHz
SPAN 200.0 kHz
* SWP 1.00 s
• PLL Phase Noise
ATTEN 10 dB
RL – 5.0 dBm
ΔMKR – 53.00 dB
2.23 kHz
73.0 dBc/Hz
Ta = +25°C
CENTER 810.42500 MHz
*RBW 100 Hz VBW 100 Hz
SPAN 20.00 kHz
* SWP 3.00 s

*(Continued)*

*(Continued)*


PLL Lock Up Time
810.425 MHz → 826.425±1 kHz
Lch → Hch 1.40 ms
850.00500 MHz
10.00000 Hz/div
810.00000 MHz
5.0000000 ms
PLL Lock Up Time
826.425 MHz → 810.425±1 kHz
Hch → Lch 1.52 ms
860.00000 MHz
10.00000 Hz/div
810.00000 MHz
5.0000000 ms
830.00500 MHz
2.00 KHz/div
829.99500 MHz
5.0000000 ms
830.00500 MHz
2.00 KHz/div
829.99500 MHz
5.0000000 ms

## ■ APPLICATION EXAMPLE




VP: 5.5 V Max

Notes:
- SSOP-16
- In case of using a crystal resonator, it is necessary to optimize matching between the crystal and this LSI, and perform detailed system evaluation. It is recommended to consult with a supplier of the crystal resonator. (Reference oscillator circuit provides its own bias, feedback resistor is 100 kΩ (typ).)

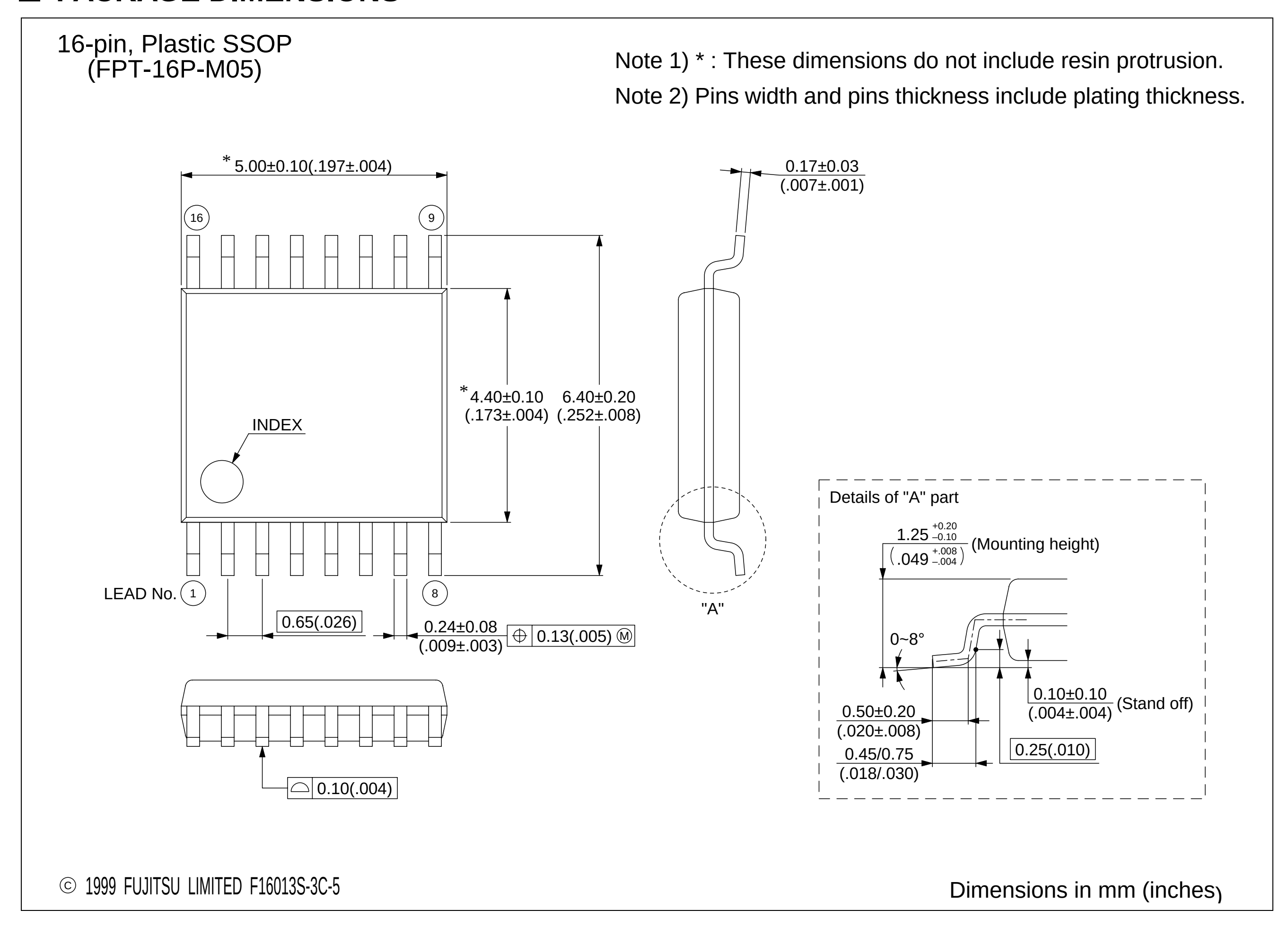
## ■ USAGE PRECAUTIONS

To protect against damage by electrostatic discharge, note the following handling precautions:
-Store and transport devices in conductive containers.
-Use properly grounded workstations, tools, and equipment.
-Turn off power before inserting device into or removing device from a socket.
-Protect leads with a conductive sheet when transporting a board-mounted device.

## ■ ORDERING INFORMATION

| Part number | Package | Remarks |
|---|---|---|
| MB15E03SLPFV1 | 16-pin, Plastic SSOP (FPT-16P-M05) | |
| MB15E03SLPV1 | 16-pad, Plastic BCC (LCC-16P-M06) | |

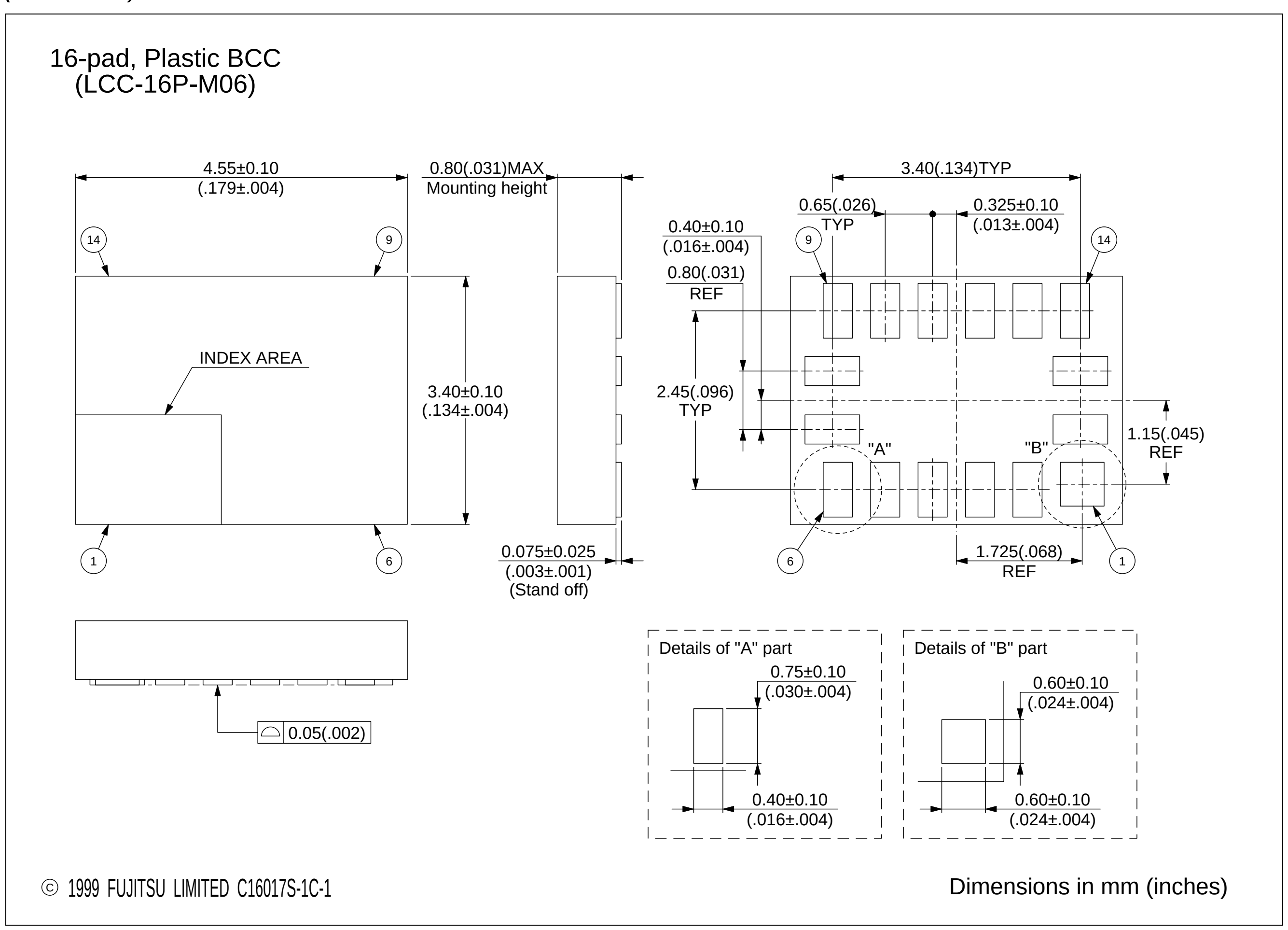
## ■ PACKAGE DIMENSIONS






*(Continued)*

*(Continued)*


16-pad, Plastic BCC
(LCC-16P-M06)
4.55±0.10
(.179±.004)
0.80(.031)MAX
Mounting height
3.40(.134)TYP
0.65(.026)
TYP
0.325±0.10
(.013±.004)
0.40±0.10
(.016±.004)
0.80(.031)
REF
14
9
INDEX AREA
3.40±0.10
(.134±.004)
2.45(.096)
TYP
1.15(.045)
REF
"A"
"B"
1
6
0.075±0.025
(.003±.001)
(Stand off)
1.725(.068)
REF
0.05(.002)
Details of "A" part
0.75±0.10
(.030±.004)
0.40±0.10
(.016±.004)
Details of "B" part
0.60±0.10
(.024±.004)
0.60±0.10
(.024±.004)
Dimensions in mm (inches)

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